REMARKS

Claims 1-7 and 9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Cherne, *et al.* (U.S. Statutory Invention Registration No. H1435). Claims 8 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cherne, *et al.* In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed and reconsideration of the rejections is requested.

Rejected claims 1-10 have been cancelled. Accordingly, the rejections of the claims are overcome. New claims 18-36 are added herewith. New claim 18 sets forth source and drain regions of the applicants' claimed semiconductor device having a symmetrical structure. New claims 28-36 recite the body contact region of the device not overlapping the gate conductive layer of the device. Neither of these features are taught or suggested by Cherne, *et al.* Accordingly, it is believed that the new claims are allowable over Cherne, *et al.*

With regard to claims 18-27, in Cherne, *et al.*, a N+ source and an N+ drain are asymmetrical structures. The Examiner is referred to column 5 lines 18-23 and Figures 9 and 10 of Cherne, *et al.* wherein the asymmetrical source and drain structures are disclosed. In contrast, referring to Figure 2A of the present application, source and drain regions 130, 140 of the applicants' invention are symmetrical structures. The symmetrical nature of the source and drain regions of the applicants' device are set forth in the new claims 18-27 submitted herewith. Cherne, *et al.* neither teach nor suggest the features of the invention set forth in the new claims. Accordingly, it is believed that the new claims are allowable over Cherne, *et al.*

With regard to claims 28-36, referring to Cherne, *et al.*, P+ and portions 71 and 72 overlap an N+ source (see Figure 9 of Cherne, *et al.*) As a result, the channel width is narrowed and the amount of current flow decreases. In contrast, in the present invention, a P+ body contact region 160 does not overlap with the N+ source 130 (see Figure 2A of the application). Similarly, in Cherne, *et al.*, the P+ and portions 71 and 72 overlap a polysilicon gate 21 (see Figure 9 of Cherne, *et al.*). However, in the present invention, the P+ body contact region 160 does not overlap the gate conductive layer 200. New claims 28-36 specifically recite this feature of the invention, namely, that the body contact region does not overlap the gate conductive layer.

Accordingly, Cherne, *et al.* neither teach nor suggest the invention set forth in new claims 28-36. Therefore, it is believed that new claims 28-36 are also allowable over Cherne, *et al.*.

Attached hereto is a marked-up version of the changes made to the claims and specification by the current Amendment. The attached page is captioned "Version with Markings to Show Changes Made".

In view of the amendments to the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Version with Markings to Show Changes Made

In the claims:

The following new claims have been added:

18. (New) A semiconductor device having a silicon-on-insulator (SOI) structure, comprising:

an insulating layer;

an insular silicon region having first conductivity-type impurity ions formed on the insulating layer;

a source region having second conductivity-type impurity ions formed at an end of the insular silicon region;

a drain region having second conductivity-type impurity ions spaced apart from the source region at the other end of the insular silicon region;

an insular body region formed in the insular silicon region, the insular body region being disposed between the source and drain regions, a channel being formed on the insular body region;

a body contact region having first conductivity-type impurity ions, the body contact region being in contact with and connected to the source region and the insular body region;

a conductive layer formed on the source region and the body contact region; and

a source electrode connected to the body contact region,

wherein the source and drain regions have a symmetrical structure.

19. (New) The semiconductor device of claim 18, wherein the body contact region is

formed on one side of the source region.

20. (New) The semiconductor device of claim 18, wherein the body contact region is formed on both sides of the source region.

21. (New) The semiconductor device of claim 18, wherein the insulating layer is an oxide layer.

22. (New) The semiconductor device of claim 18, wherein the insular silicon region is a single crystal silicon layer.

23 (New) The semiconductor device of claim 18, further comprising:
a gate insulating layer formed on the insular body region;
a gate conductive layer formed on the gate insulating layer;
a gate electrode electrically connected to the gate conductive layer; and
a drain electrode electrically connected to the drain region.

24. (New) The semiconductor device of claim 18, wherein the conductive layer is a salicide layer.

25. (New) The semiconductor device of claim 24, wherein the salicide layer is one of a cobalt salicide layer, a titanium salicide layer, and a nickel salicide layer.

26. (New) The semiconductor device of claim 18, wherein the first conductivity-type impurity ions are p-type and the second conductivity-type impurity ions are n-type.

27. (New) The semiconductor device of claim 18, wherein the first conductivity-type

impurity ions are n-type and the second conductivity-type impurity ions are p-type.

28. (New) A semiconductor device having a silicon-on-insulator (SOI) structure, comprising:

an insulating layer;

an insular silicon region having first conductivity-type impurity ions formed on the insulating layer;

a source region having second conductivity-type impurity ions formed at an end of the insular silicon region;

a drain region having second conductivity-type impurity ions spaced apart from the source region at the other end of the insular silicon region;

an insular body region formed in the insular silicon region, the insular body region being disposed between the source and drain regions, a channel being formed on the insular body region;

a gate insulating layer formed on the insular body region;

a gate conductive layer formed on the gate insulating layer;

a body contact region having first conductivity-type impurity ions, the body contact region being in contact with and connected to the source region and the insular body region;

a conductive layer formed on the source region and the body contact region; and

a source electrode connected to the body contact region,

wherein the body contact region is not overlapped with the gate conductive layer.

29. (New) The semiconductor device of claim 28, wherein the body contact region is formed on one side of the source region.

30. (New) The semiconductor device of claim 28, wherein the body contact region is formed on both sides of the source region.

31. (New) The semiconductor device of claim 28, wherein the insulating layer is an oxide layer.

32. (New) The semiconductor device of claim 28, wherein the insular silicon region is a single crystal silicon layer.

33. (New) The semiconductor device of claim 28, wherein the conductive layer is a salicide layer.

34. (New) The semiconductor device of claim 33, wherein the salicide layer is one of a cobalt salicide layer, a titanium salicide layer, and a nickel salicide layer.

35. (New) The semiconductor device of claim 28, wherein the first conductivity-type impurity ions are p-type and the second conductivity-type impurity ions are n-type.

36. (New) The semiconductor device of claim 28, wherein the first conductivity-type impurity ions are n-type and the second conductivity-type impurity ions are p-type.